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# The Smart Frame Buffer Goes Hollywood: 3D and TV

**Starring**
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**Western Research Laboratory**

**Not starring**
**Bob McNamara**
**Chris Gianos**
**Too Chicken to Give Talks Group**

**Digital Equipment Corporation**

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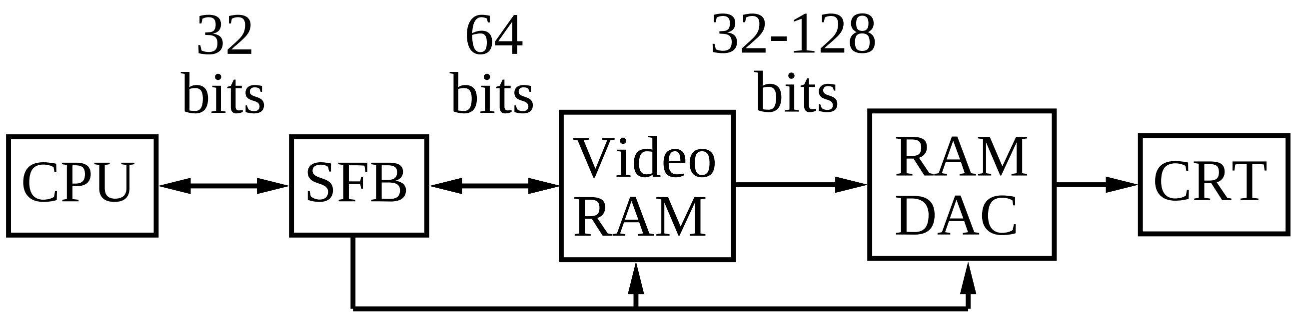
# A Short History of the Sfb: Why?

Dumb color frame buffer okay for MIPS pmax, but...

- Alpha AXP didn’t have byte writes
- 3max graphics at end of slow TURBOchannel
- Cfb performance lagging industry

# A Birds-Eye View



# A Short History of the Sfb: Philosophy

- CPU does flow control, sfb does pixel painting
- One command paints at most 32 pixels
- No command takes longer than a bus timeout

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# Why Another Chip?

Performance:

- HP 730 with CRX graphics accelerator is faster on lines, large solid fills, and most copies
- Bob said we could do 2x HP line rate
- Number 2 stinks

3D:

- Can we provide respectable performance with really cheap graphics hardware?

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# Sfb+ Enhancements

Higher Peformance:

- Faster clock rate (from 40 nsec to 26.3)
- New memory architecture for fast lines
- VRAM block fill mode for solid, stippled, and tiled areas
- DMA pixel data for live video

New Functionality:

- 3D shading, Z-buffering, stencil buffering, multibuffering

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# Sfb+ Modes of Operation

- (Mostly) dumb frame buffer
- Transparent stipple
- Opaque stipple
- Block stipple
- Transparent, opaque, and block stipple fill
- Copy pixels
- DMA pixels
- Line drawing

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# Philosophy Behind Accelerated Modes

Set sfb+ mode.

Set up a few registers (foreground, background, etc).

Start writing 32-bit data words to frame buffer.

- Destination address points somewhere into screen memory.
- Each data bit specifies what happens to one pixel.

Sfb+ violations:

- DMA and stipple fill modes may affect up to 2048 pixels per 32-bit command.

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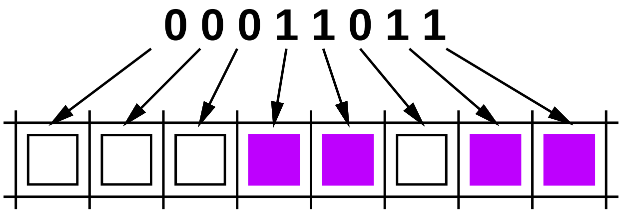
# Transparent Stipple Mode

Transparent stipple expands 32 data bits to pixels:

- 0 means do nothing
- 1 means use the foreground pixel




For solid fill, use a data word of all 1's.

Use 0 bits at left and right edges of span for ragged (non-aligned) edges.

Paints 64 bits every 2 clock ticks.

In block fill mode, VRAMs do transparent stipple semantics at 32 bytes every 2 clock ticks.

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# Line Memory Architecture

How to draw lines 3x faster than sfb:

- Sfb+ clock is 26.3 nsec, sfb was 40 nsec
- Sfb+ generates line pixel every tick, sfb was every two ticks.
- Memory system architecture retires pixels (almost) as fast as they are generated.
- Better performance than HP's Hummingbird, even though we clock memory less aggressively.

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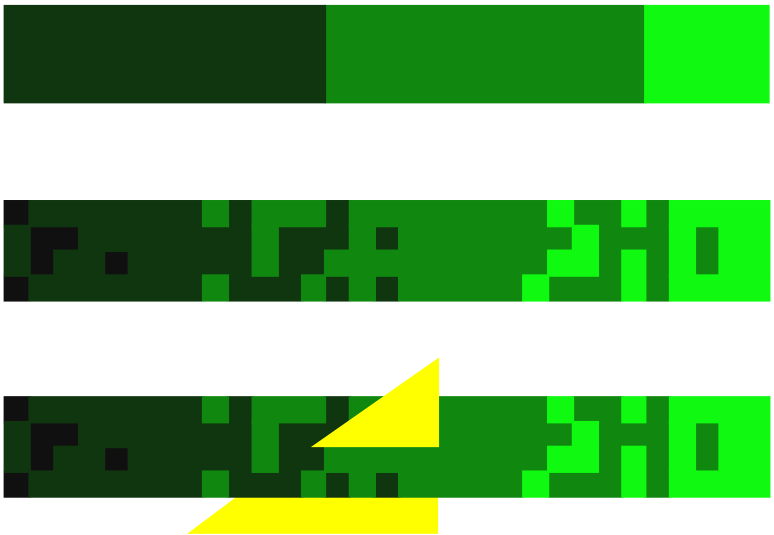
# New Functionality for 3D

- Sfb+ lines can be:

Shaded

Dithered

Z-buffered



- 8/8/8 and 12/12 in-place double-buffering
- Stereo viewing
- 8-bit windows don’t slow down on 24-plane system

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# Performance Comparisons

Cfb on an ancient 3max+ DECstation @ 40 MHz.

Sfb on Flamingo II @ 200 MHz.

CRX on HP 730 (CRX48Z is faster and more expensive, but we don't have numbers.)

Sfb+ on Flamingo II @ 200 MHz.

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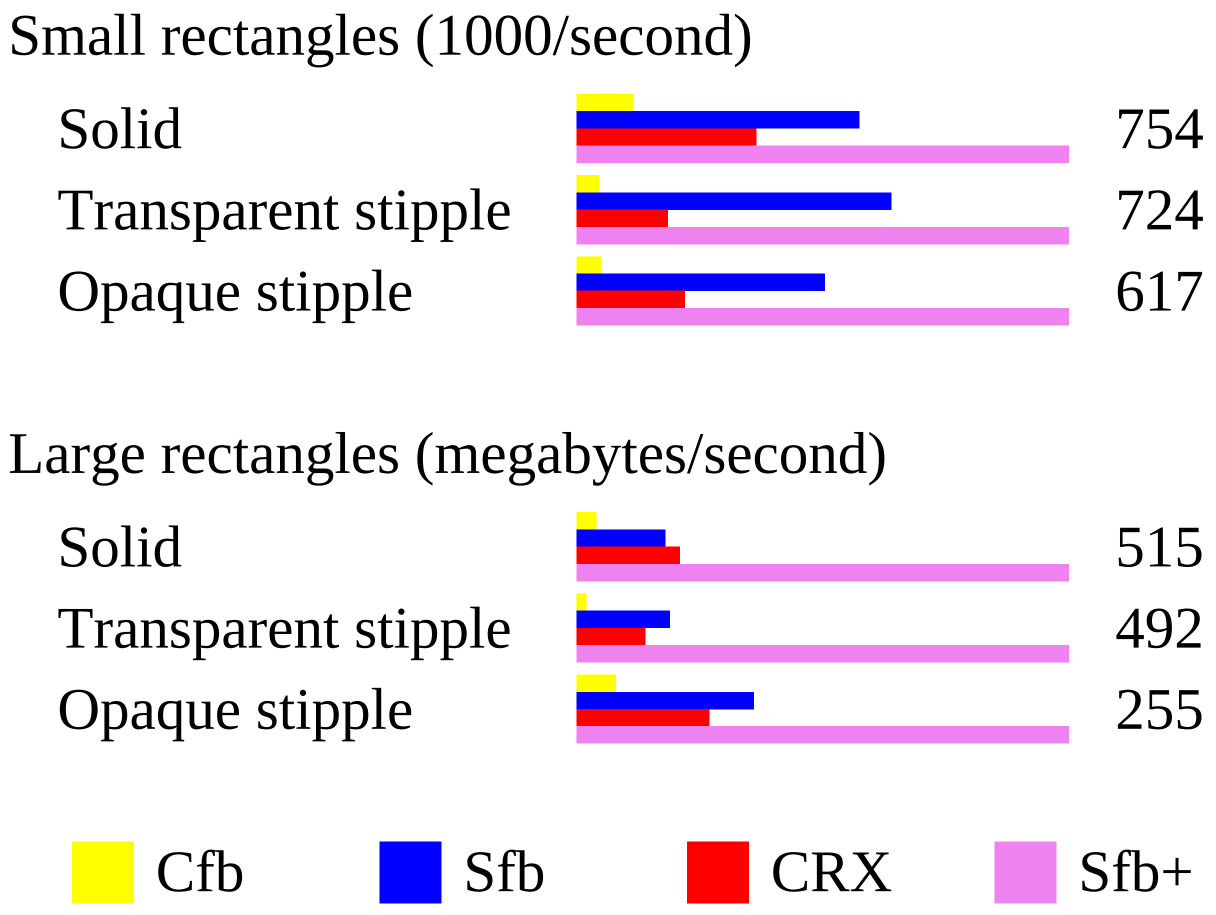
# Rectangle Fill Performance

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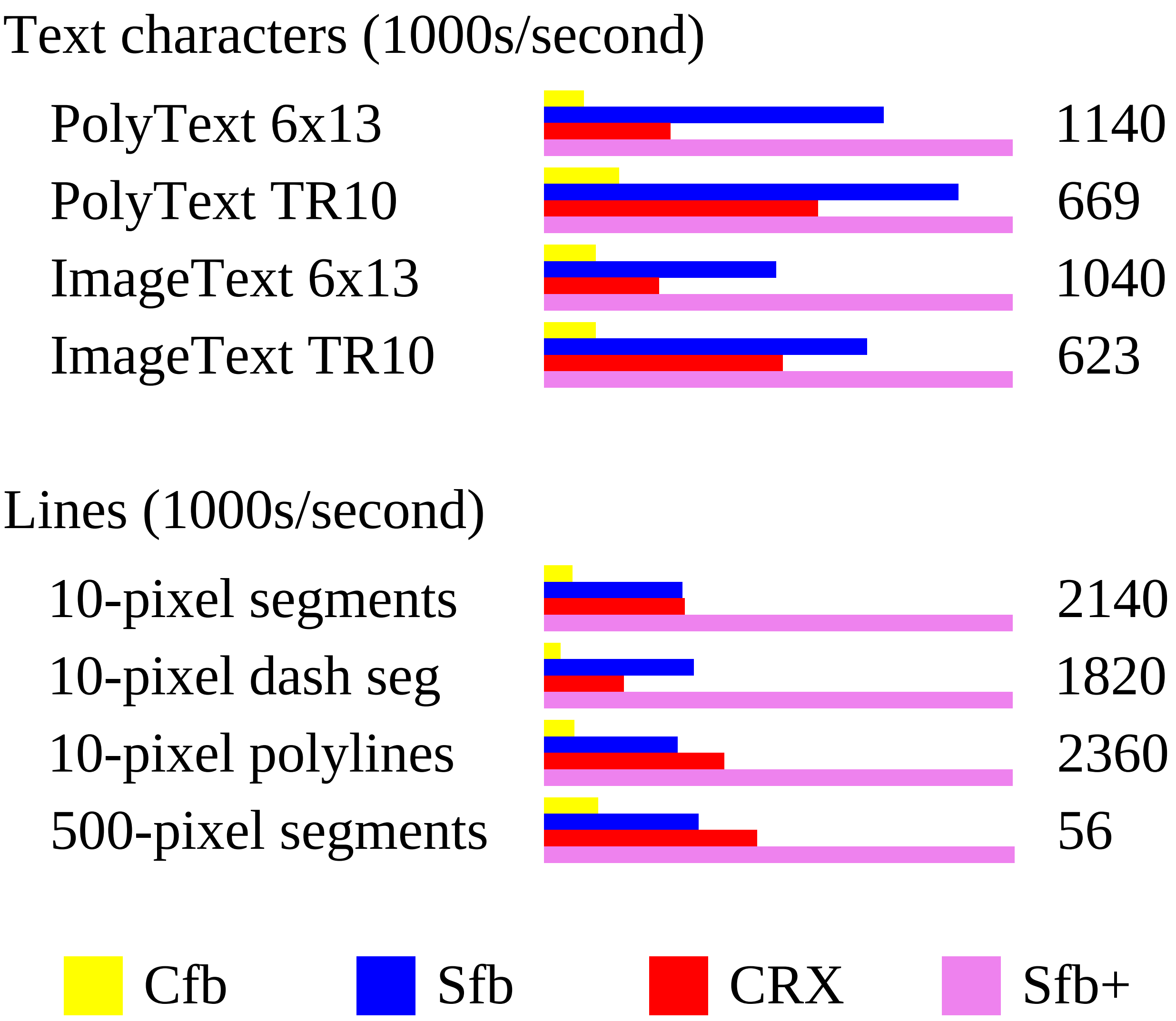
# Character and Line Performance

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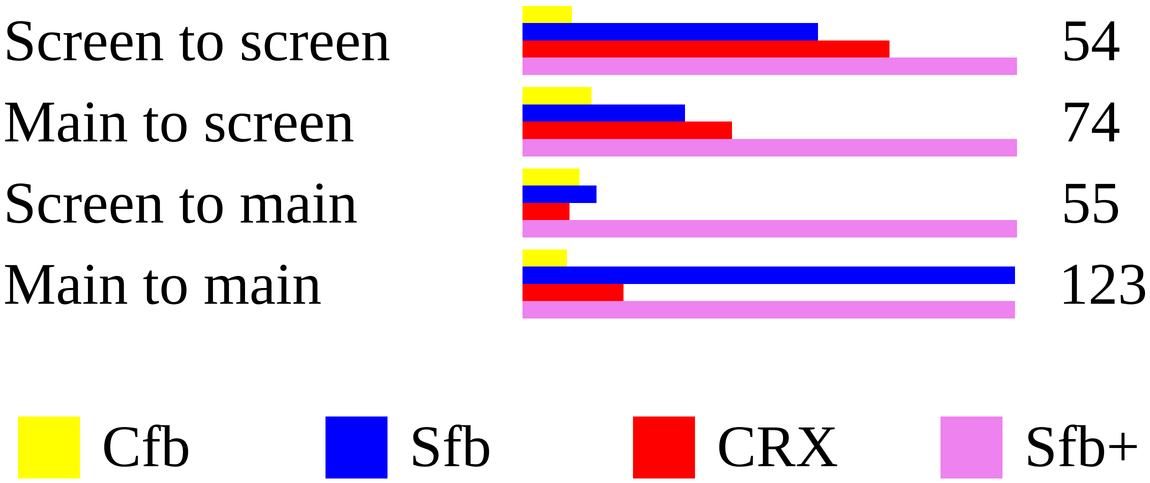
# Copy and DMA Performance

Copy large areas (megabytes/second)

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# Conclusions

- Memory bandwidth is usually the limiting factor to 2-D graphics performance.
- A simple smart frame buffer increases bandwidth over a dumb frame buffer, and increases small-scale parallelism.
- Software does yucky control flow using cfb-like algorithms.
- World-class 2D performance, good low-end 3D performance.

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# References

No paper yet on sfb+, but:

- WRL Research Report 91/1, ‘‘Writing Fast X Servers for Dumb Color Frame Buffers’’
- WRL Research Report 93/1, ‘‘A Smart Frame Buffer’’

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